Early-Stage RTL Power Estimation and Exploration

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***Abstract*—Power management strategies, which were once used for a few applications, have become ubiquitous. Based on Moore's Law, the number of transistors on a microchip doubles every two years, emphasizing the importance of early-stage power exploration. Designers can no longer hold up until the end-most netlist to get accurate power numbers. Estimating power consumption early in the design process is imperative to tackle these issues. This paper addresses the problem of robust early estimation of power since visibility is needed from the start of register transfer level (RTL) coding. Voltage domains, switchable power domains, and clock-gating techniques are examples of common power-saving approaches. Although voltage and power domains necessitate unique logic circuits and complicate power grid architecture, it is necessary to ensure that they are adequately met. The power estimation and exploration solution aid in estimating data across different intellectual properties (IPs) and circuits. These configurations entail conducting power estimates, profiling, and reduction iteratively to assess and enhance the power efficiency of the design. This paper aims at finding the significant power loopholes at the preliminary stage of the RTL, a time when the most rewarding modifications can be made, thereby saving both power and overall turnaround time.**

***Index Terms*—Average Power, Clock Gating, Low-Power Design, Power Exploration, RTL**

I. INTRODUCTION

Every milliwatt of power counts, regardless of the application. The overall power of a Silicon on Chip (SoC) architecture is mainly composed of its dynamic and static power components. Dynamic power is the amount of power utilized by a device as the signals vary. The dynamic power sources required during logic changes on nets are switching power and internal power. The switching power is the energy used to charge and discharge the output net's capacitance. When switching, the power dissipated inside the gate is internal (short circuit power/crowbar power). Static power is associated with the power dissipated when the transistor is in an idle state. Static power is also referred to as "leakage power" since static power consumption in complementary metal-oxide-semiconductor (CMOS) device is primarily caused by leakage. The Low-power design can be studied at different levels, including the logic, circuit, device levels, and system architecture. In comparison, high-level optimizations necessitate in-depth research into a given application. Any low-power technique can be applied to basic digital systems at the circuit level. Power island, clock gating, transistor resizing, operating in the sub-threshold regime, multi-threshold CMOS (MTCMOS), variable threshold CMOS (VTCMOS) and different leakage power reduction strategies such as utilizing a sleep transistor, forward/reverse body biasing (FBB/RBB) are only a few examples of generic low power design methods. By reducing switching activity, clock gating approaches save power [2].

This paper provides a power estimation solution that maps the RTL design onto a gate netlist using a fast and accurate area-based synthesis engine. In the view of the fact that the engine can utilize most of the cells in the given target libraries, it can provide a reliable starting point for power calculation. The analysis in this research has been done on the dual data rate physical interface (DDR-PHY) IP. The memory IP has been shown in Fig. 1. The PHY can operate in various modes depending on the input/output ports.

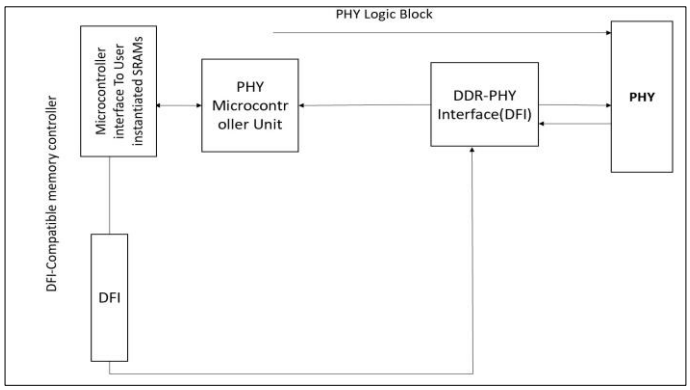

Fig. 1. A high-level diagram of DDR-PHY

The power-estimation findings were derived using the default parameters of the synthesis tools from the studies found in the literature [7]. As mentioned, components of power (1) are Static (Leakage) Power (2) and Dynamic Power (3):

$$P\,(Total) = P\,(Static) + P\,(Dynamic) \quad (1)$$

$$P\,(Static) = I{*}V \quad (2)$$

$$P\ (Dynamic) = C_L * V^2 * \alpha * f \quad (3)$$

where: I is the current, V is the supply voltage, C_L is the load capacitance, f is the frequency of operation and α is the activity factor (0 to 1).

The number of operations when a capacitive load is charged and discharged is determined by the switching activity and the frequency of operation. These design properties can be applied at any abstraction level, and they must be aligned. The power exploration process improves the clock gating ratio (CGR) and clock gating efficiency (CGE). There are four critical components for estimation and reduction, as indicated in Fig. 2, to tackle all elements of power analysis, including early RTL estimation and exploration [3].

- Power Estimate
- Power Exploration
- Power Reduction
- RTL Power Sign-Off

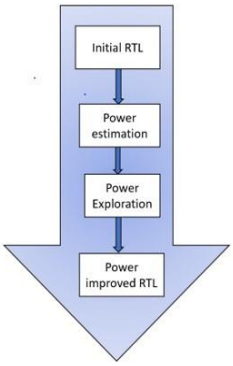

Fig. 2. Flow diagram for power estimation and reduction

II. PROBLEM STATEMENT

The power analysis' goal is to examine every watt. As shown in Fig. 3, the study here is restricted to the low power state of PHY. PHY Fast Standby/Low Power (LP2) allows the SoC to save the maximum power while the DRAM is in a Self-Refresh mode. Fig. 3 shows the output of the circuit under design that uses the following constraints:

- Interface Protocol: DFI
- Clock name: clock
- Status Interface Signal: DFI start
- Status Interface Signal: DFI complete

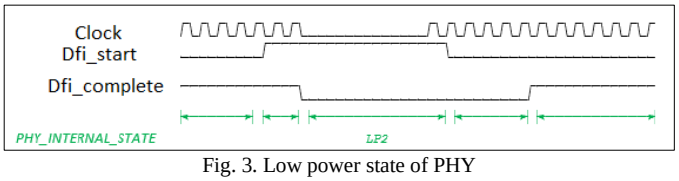

Fig. 3. Low power state of PHY

As the LP2 stage expects to have the maximum power saving, it is required to maintain a low power criterion. This problem, indeed, will not be achievable by the conventional methods of power estimation as it requires a finalized netlist. However, waiting for the stable RTL for the LP2 stage raised concerns about the turnaround time and expectations led to the notion of RTL power exploration at an early stage [6],[8]. The results of the Early-Stage RTL in Fig. 4, on the other hand, exceed the power specifications. The efficacy of the developed RTL is achieved by analysing every statistical element of RTL. Since a design's power is a consequence of how it conducts a calculation over time, practically all of the crucial alterations that significantly impact a design's power are sequential—they alter the sequence of values created at key internal registers or memories over time.

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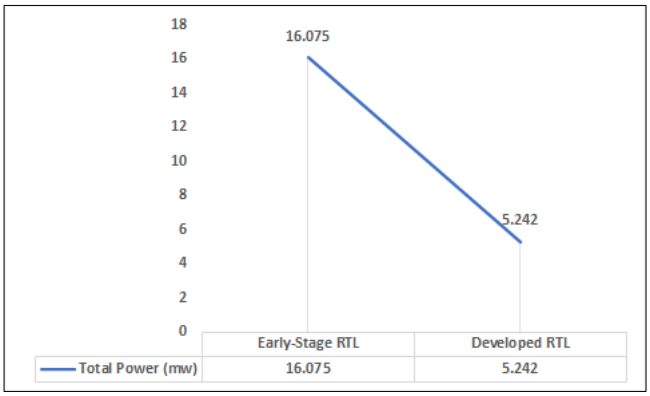

Fig. 4. Power estimates at different RTL stages

A. POWER REDUCTION METHODOLOGY

The second synthesis design proposed here aims to apply power optimizations to the different implementation techniques. All the components of the design are inferred and synthesized for maximum performance.

Activity:

Time versus Activity filters out crucial time stamps, allowing for more accurate power analysis. Fig. 5 aids in selecting suitable intervals for power analysis and ensures that the test benches have adequate functional coverage. The highest and lowest activity levels are of relevance.

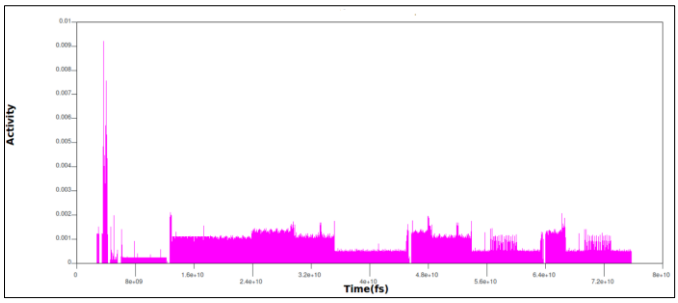

Fig. 5. Time versus Activity graph

Power Reduction:

The design information of all underlying hierarchies is analysed. The proposed design attributes for early-stage power exploration are:

- Design/Block Status
- Annotation Status
- Clock Gating Status
- Register Gating Status
- Gating type

A pie-chart shown in Fig. 6 helps identify the loopholes in a better way [4]. The mentioned components have different roles in power estimation and reduction for proper visualization. A series of processes were carried out to get to the stated power levels.

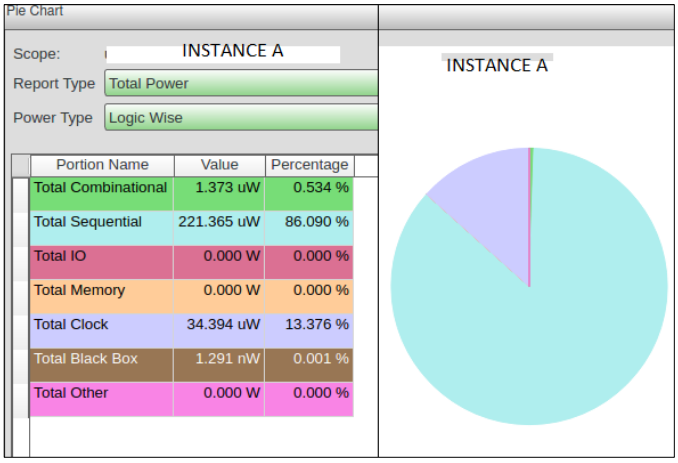

Fig. 6. Power distribution across different logic blocks

Clock gating regression was done to identify gating opportunities across multiple simulation files [5]. Hierarchies with poor clock gating, poorly gated registers, and memories were identified. Few of the parameters are stated in Fig. 7 (a) and (b).

Instance Heirarchy	Average Register D Pin Activity	Average Activity	Average Clock Pin Activity	Average Driving Clock Activity
local_logic	0.015	0.015	0.415	1.100
local_logic_1	0.000	0.015	0.175	0.507
local_logic_2	0.049	0.034	0.714	0.985
local_logic_3	0.049	0.033	0.714	0.985
local_logic_4	0.036	0.017	0.714	0.985
local_logic_5	0.051	0.031	0.714	0.985
local_logic_6	0.029	0.019	0.571	0.854
local_logic_7	0.029	0.019	0.571	0.854
local_logic_8	0.016	0.022	0.857	2.000
local_logic_9	0.015	0.021	0.857	2.000
local_logic_10	0.000	4.26E-03	0.857	2.000
local_logic_11	0.013	0.018	0.857	2.000
local_logic_12	NA	0.000	NA	NA
local_logic_13	0.000	0.013	0.516	0.532
local_logic_14	NA	0.000	NA	NA
local_logic_15	0.000	0.000	0.000	0.247

(a)

Instance Heirarchy	Average Clock Gating Efficiency (%)	Average ROADF(%)	Average ROADE(%)	Average QD(%)
local_logic	68.655	6.613	21.672	74.398
local_logic_1	65.546	0.000	4.878	NA
local_logic_2	53.333	13.469	38.159	63.618
local_logic_3	53.333	15.201	41.206	68.633
local_logic_4	53.333	3.628	6.667	94.521
local_logic_5	53.333	13.850	27.492	62.647
local_logic_6	55.814	2.965	25.581	97.203
local_logic_7	55.814	2.965	25.581	97.203
local_logic_8	57.143	3.829	3.829	100.000
local_logic_9	57.143	3.604	3.604	100.000
local_logic_10	57.143	0.000	0.000	NA
local_logic_11	57.143	2.928	2.928	100.000
local_logic_12	NA	NA	NA	NA
local_logic_13	11.111	0.000	0.000	NA
local_logic_14	NA	NA	NA	NA
local_logic_15	100.000	NA	NA	NA

(b)

Fig. 7. Hierarchical based matrix to investigate power loopholes

The following are a few of the approaches used to calculate the achievable power numbers:

Enable and clock gating:

The proposed methodology is to use an integrated clock-gating cell (ICGC). This is advantageous for designers as the power consumed by this ICGC is generally much less than the conventional re-circulating register. Fig. 8 depicts the conventional and the ICGC method. The measured power is lower because the local clock signal is less active in ICGCs. This ensures better enable and clock gating [9],[10].

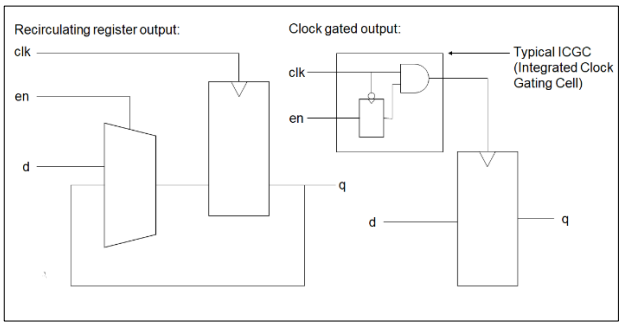

Fig. 8. Typical and ICGC topology

Mix Voltage Thresholds (Vt):

Multiple Vt levels have been used to minimize active leakage power and delays.

The library contains two or more cells with the same function, same operating voltage, different cell names, and different leakage values in this design. One variation of the cell (low Vt) is faster but has more leakage, while another variant (high Vt) is slower but has less leakage. The designer's motivation is to minimize leakage while still achieving the timing estimates.

Power Register Reduction:

The other advanced methodology is to reduce the power of the register part of the design. The vital data observed here in Fig. 9 is the Q/CP ratio, where Q denotes the output frequency and CP denotes the clock frequency. It is also termed Register

Output Activity Density per Flip-flop (ROADF). This helps identify registers for which the data is not toggling, but the clock pin is toggling.

This is also a power bug. Low Q/CP marks the need to determine a new enable or strengthen the enable of the given register. The overall ROADF versus CGE of the design has been shown in Fig 9. Further debugging can be done based on the targeted register.

CG Efficiency						
ROADF(Q/CP)	0%-0%	0%-25%	25%-50%	50%-75%	75%-100%	100%-100%
50%-100%	4	0	0	0	0	0
37.5%-50%	0	0	0	0	4	0
25%-37.5%	12	0	0	0	4	0
12.5%-25%	10	0	0	0	60	0
0%-12.5%	124	0	0	0	28	0
0%-0%	138	0	0	64	160	0

Fig. 9. Overall ROADF versus CGE

Apart from all these methods, numerous other techniques can also be exploited to save power and maximize performance. Observing these approaches, the above-mentioned methods can be employed only before the design synthesis, hence emphasizing the need for early power exploration. This flow necessitates a basic understanding of the tool by the designer.

III. RESEARCH ELABORATIONS

A. FORWARDING ANALYSIS TO DIFFERENT RTLs

It is worth mentioning that the PHY may respond differently under certain circumstances. As a result, power estimation is required in all possible power-glutton scenarios.

Considering the scenarios when PHY does normal functions such as reading, writing, and routine updates. It is ludicrous to think that consumption should be the same in all conditions. Therefore, it is critical to understand the importance of dynamic and static power in all these scenarios.

Some optimal scenarios have been developed and fed to the tool via random constrained verification to enhance the observability of power system dynamic state estimation. This work can be further investigated considering the robustness against frequencies and voltages.

Proposition 1: Consider the case where back-to-back reads happen from DFI Interface to the DRAM Interface. PHY will be executing instructions. The following Fig. 10 shows the power numbers of two different RTLs in the case of successive reads.

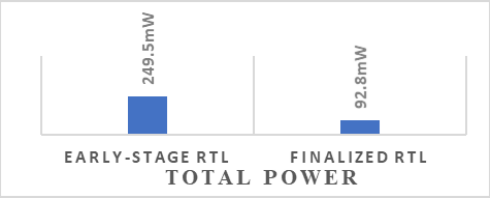

Fig. 10. Total Power for Early-Stage and finalized RTL for back-to-back reads

Proposition 2: Memory will now be executing write instructions in the context of back-to-back writes from the DFI Interface to the DRAM Interface. The following Fig. 11 shows the power numbers of two different RTLs in the case of successive writes.

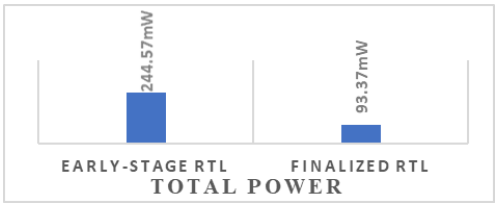

Fig. 11. Total Power for Early-Stage and finalized RTL for back-to-back writes

Proposition 3: Given that the memory is idle and does not undergo routine updates or training, it is expected to have less power than customary reads or writes. The following Fig. 12 shows the power numbers of two different RTLs in the idle case.

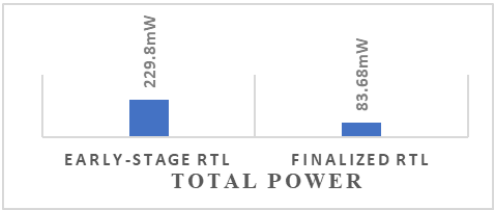

Fig. 12. Total Power for Early-Stage and finalized RTL for idle case

In the above proposed method, designer/architect can take the reference of already accomplished work as a starting building block for any enhancement in RTL.

IV. SIMULATION SOFTWARE

There is several software available that can mimic the process involved in this research work and can produce the possible result. One such type of tool is Spyglass [1]. Spyglass Power Estimation and Exploration solutions are the most capable of estimating and lowering the power of a design while it is still in the RTL stage. Spyglass receives the design via restricted random verification. It is critical to combine estimation and reduction. Spyglass Power Estimation and Exploration systems, when configured correctly, are tightly integrated and calibrated to give excellent power correlation with gate-level and silicon estimations. This is a must-have if one wants to move forward with power reduction on the design safely.

V. CASE STUDY

Fig. 4 illustrates the examination of power consumption over time in the second section. It compares the spyglass power numbers to the expected power figures. The traditional approach of measuring power at the netlist level would have resulted in several RTL changes and slowed down turnaround time. RTL had to be modified because the requested power varied significantly from actual estimates.

The third section described power flow exploration using two RTLs: an ongoing RTL that has yet to release the netlist and a stable RTL with a finalized netlist and structure. The two RTLs taken have almost similar functionalities and structures for comparison.

The first design is a functional design that will be improved in the future. The second design has a more enhanced, pipelined, and unvarying flow. The development cycle becomes crystal clear by comparing the outcomes of the ongoing design to the stable design. Designers will get the power numbers to compare and analyse the design's power requirements. As a result, any major or minor changes can be made considering power numbers.

VI. RESULTS

The power numbers presented in this paper results from thorough verification in all possible operational modes simulated at TSMC 5nm technology node. Power estimation, exploration and reduction have been performed on several subcategories. Different categories are considered for low power design, including memories, latches, I/O pads, flops, clocks, and other sub-sections. Fig. 13 depicts a power report of the LP2 stage stated in the Problem Statement using a line chart. Frequency, operating voltage and constraints are kept the same for comparison purpose.

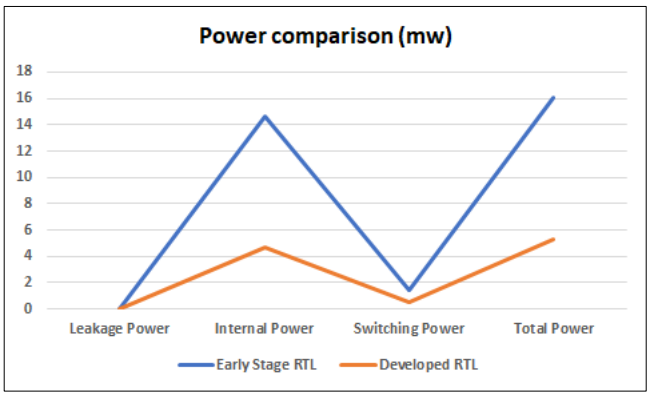

Fig. 13. Power comparison between the two stages of RTL

Similarly, power distribution is monitored continuously at subsequent stages of the development cycle, and hence the best performing RTL is achieved. Investigating all the power components, we obtain the figures in Table I for the LP2 stage.

After analysing and inspecting all power components from section 3, the figures in Table II, Table III and Table IV, for the various modes of operation are obtained. The RTLs were subjected to the same environmental constraints for comparison.

TABLE I. POWER NUMBERS BETWEEN TWO STAGES OF RTLs

Power Components	**Early Stage RTL/(mw)**	**Developed RTL/ (mw)**
Leakage Power	0.022	0.022
Internal Power	14.623	4.680
Switching Power	1.429	0.539

TABLE II. POWER ESTIMATES BETWEEN TWO DIFFERENT RTLs FOR BACK TO BACK READ MODE

Power Components	**Early Stage RTL/(mw)**	**Developed RTL/ (mw)**
Leakage Power	0.041	0.022
Internal Power	213.688	80.407
Switching Power	35.852	12.383

TABLE III. POWER ESTIMATES BETWEEN TWO DIFFERENT RTLs FOR BACK TO BACK WRITE MODE

Power Components	**Early Stage RTL/(mw)**	**Developed RTL/ (mw)**
Leakage Power	0.041	0.022
Internal Power	210.429	81.096
Switching Power	34.104	12.259

TABLE IV. POWER ESTIMATES BETWEEN TWO DIFFERENT RTLs FOR IDLE MODE

Power Components	**Early Stage RTL/(mw)**	**Developed RTL/ (mw)**
Leakage Power	0.041	0.022
Internal Power	200.078	73.775
Switching Power	29.717	9.891

VII. CONCLUSION

This work presents a comprehensive method that addresses all elements of power analysis, including early RTL estimate and exploration, by using the RTL Spyglass signoff tool. This delivers meaningful feedback regarding the design architecture from a low power perspective at the RTL stage in a user-friendly manner. This process can be standardized and included as an add-on feature in simulators by verification teams. This methodology allows design teams to create the Spyglass Power log file for each accompanying RTL module.

The proposed methodology is most effective before synthesis, as every decrease in process geometry makes power targets hard to achieve. This paper presents a novel methodology to compare RTL sequential stages. By comparison and examining already accomplished RTL with the ongoing RTL, time-to-market will be drastically reduced, also making it power efficient. Power verification may be made even more innovative and more intelligent this way, allowing for a faster turnaround time.

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