A Novel Simulation Flow for 7nm Mixed-Signal Design Transistor Level Verification

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Abstract: A single simulation environment for both analog and digital circuits is developed. A new parallel simulator is utilized to perform functional verifications at transistor level. The efficiency of the flow is demonstrated using a PLL top-level testbench. This flow is proven efficient to detect potential bugs at an early design phase.

I. INTRODUCTION

Mixed-signal design and verification become increasingly challenging at 7nm and below, especially for digital and analog co-simulations. Advanced yet complicated device models and enlarged circuit size lengthen the simulation time and heighten the demand for computation resource. Complex chip architectures with a high degree of functional block integration require extensive verification coverage. Due to the large scope of analog and digital circuitries, mixed signal co-simulation is traditionally run at a higher level where the digital part is simulated with a digital simulator and the analog part with a fast SPICE simulator. One issue associated with this flow is that the fast SPICE simulator cannot achieve adequate accuracy required for high frequency components in analog circuits. Another issue is that in this flow the designer needs to switch back and forth between the command-line based environment for mixed-signal circuits and the schematic GUI based environment for analog circuits.

To address these challenges, we developed a new simulation flow using a single simulator in a single simulation environment. In this flow, both analog and digital circuits are simulated at the transistor level with a high-performance analog SPICE simulator. Benefitting from the simulator's high simulation throughput and low resource consumption, the simulation time is greatly reduced while the SPICE-level accuracy for analog components is maintained. Moreover, both analog schematics and digital blocks are imported into the same analog design environment where the simulation is set up and performed, eliminating the need of switching between different environments.

In this paper, we demonstrate the efficiency of our flow using a PLL top-level verification testbench. PLL is known to be one of the most challenging cases in transistor level simulation due to two reasons. First, it takes microseconds for the PLL loop to converge, leading to long simulation time. Second, the voltage-controlled oscillator (VCO) in the PLL operates at extremely

high frequency and thus requires fine simulation time steps in the picosecond range. We show that using the new flow a simulation of ~10μs successfully completes within one week. The new flow is proven efficient for functional verification and for detecting potential issues at early design phase. It enables comprehensive verification coverage, reduces design cycles, and provides confidence for final design sign-off.

II. TRADITIONAL AMS SIMULATION FLOW

The traditional AMS flow from Xilinx/AMD is illustrated in Fig. 1. It is based on a fast SPICE simulation tool and uses a command-line flow to perform verification tasks. A SPICE netlist is created from a schematic to represent analog blocks. The analog on the top test bench is created manually in the SPICE format. This flow combines the RTL Verilog code for digital blocks, SPICE netlist, and Verilog A code for analog blocks. A traditional fast SPICE engine is used for the analog simulation, and a digital engine is used for digital simulation. The output database is viewed using a waveform viewer to check simulation results.

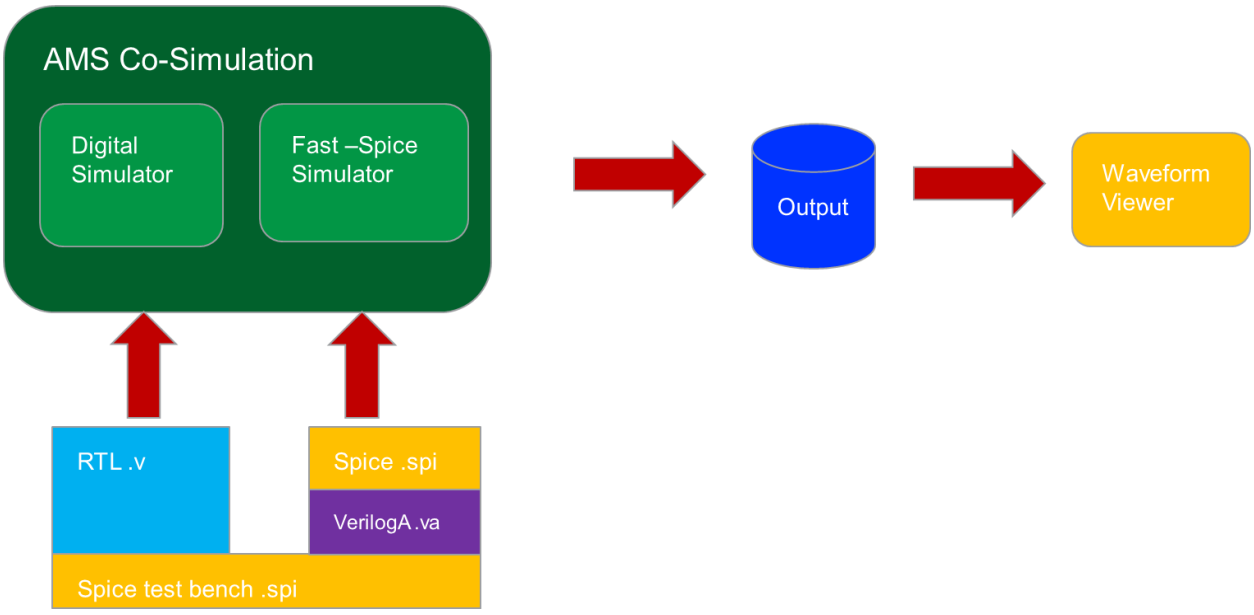


Figure 1. The Xilinx/AMD traditional AMS flow.

In this traditional flow, VCO is represented by behavioral model. As such a model may not accurately capture the real VCO's functionalities, bugs could be left undetected in design verification. An alternative approach to improve the VCO simulation accuracy is to use SPICE models to represent the component. Unfortunately, due to the complexity of distributed models inside the VCO SPICE netlist, it takes the fast SPICE tool up to months to complete the simulation,

rendering this approach neither efficient nor accurate. At 7nm and below, a new simulation flow is needed to speed up VCO simulation while maintaining good accuracy.

III. NEW AMS SIMULATION FLOW

A novel AMS flow, illustrated in Fig. 2, is developed at Xilinx/AMD for 7nm designs. This flow allows designers to use the same verification environment, the Xilinx/AMD analog design environment, for analog block level simulation as well as for higher level mixed-signal verification. In this flow, the digital RTL code is either imported into schematic or imported as an external SPICE file into the analog design environment. Then the netlist is assembled for both analog and digital blocks at the transistor level, and simulation tasks are performed, both in this environment.

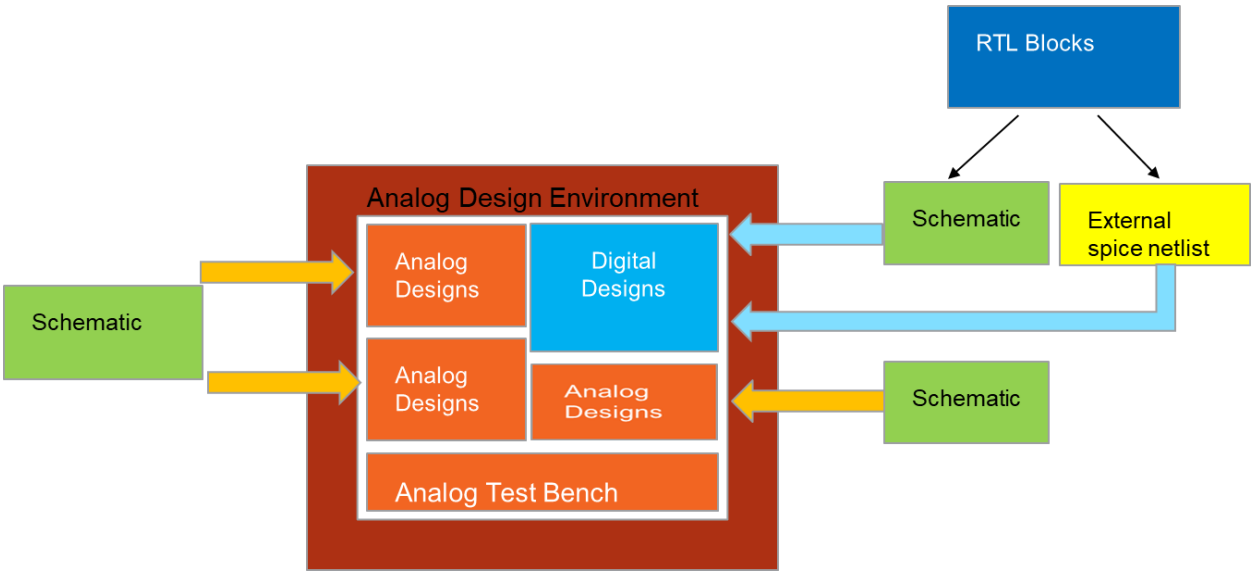


Figure 2. The new AMS simulation flow.

The importing of RTL blocks into schematics or external SPICE files is handled by the IP releasing flow, which is shown in Fig. 3. We use an industry utility to convert Verilog into cdl format and output cdl netlist. User also has the option to import RTL into OA schematic for smaller digital designs. For larger digital designs that are too big to import into OA schematic, we provide in-house flow Xilinx multi-thread netlister (xmtnetlist) to recursively walk through the design hierarchy and build the complete SPICE netlist. Xmtnetlist traverses down the digital design hierarchy and investigates OA definitions for each block, the so-called stub in the IP releasing flow, to search for those represented by cdl. After identifying all cdl stubs, xmtnetlist uses another internal utility to assemble the cdl netlists found, merge/concatenate the design definitions hierarchically, and

write out a single consolidated SPICE netlist. Xmtnetlist also runs final QA checks on the output netlist to ensure that it is clean for downstream consumption.

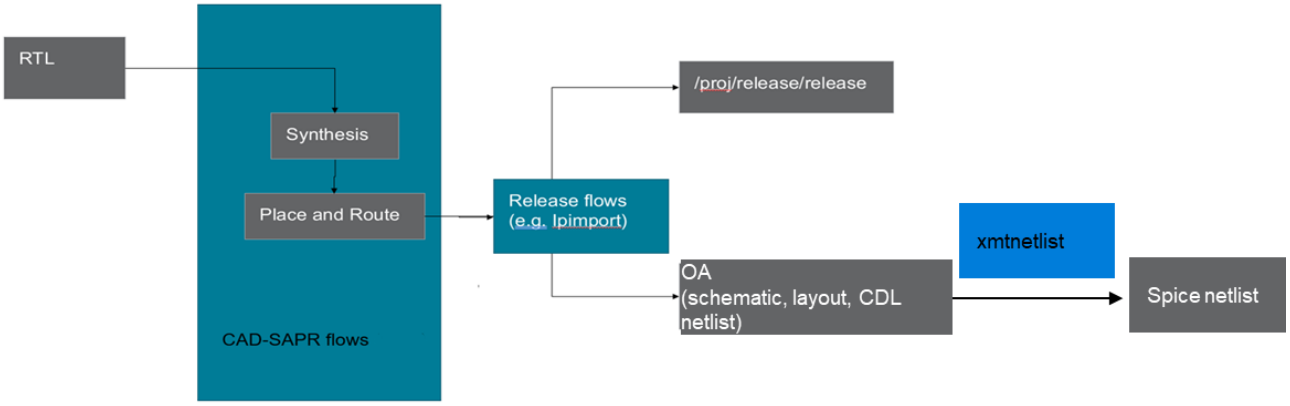
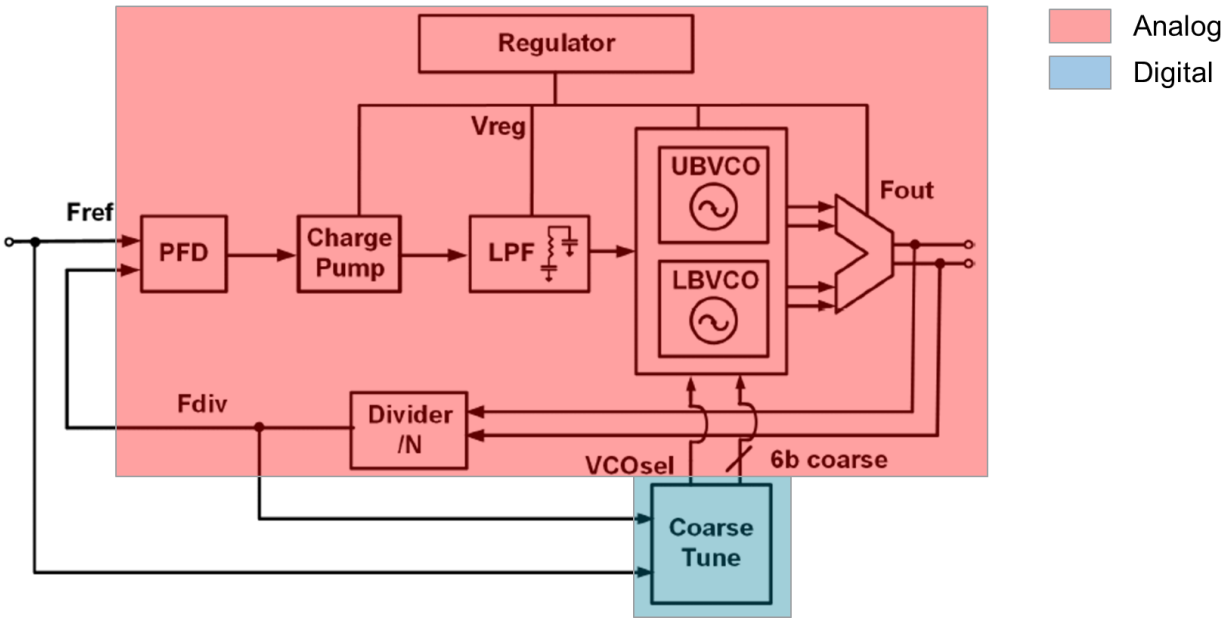


Figure 3. The IP release flow.

To speed up simulation and maintain good accuracy, a high-performance analog SPICE simulator is used as the verification engine in the new AMS flow. The simulator provides much faster simulation speed and smaller memory usage owing to its massive and scalable parallel capability especially in advanced nodes like 7nm. We adopted the VX verification mode for higher level verification. In this mode the simulator delivers even faster performance and yet achieves better accuracy than fast SPICE engines currently used do.

IV. CASE STUDY OF LCPLL

As shown in Fig. 4, LCPLL [1] used in the study is a typical PLL circuit consists of VCO, frequency divider, PFD, charge pump, and loop filter. The VCO output is fed into the frequency divider, which generates the divide down clock that is sent to PFD. PFD compares the phase of the input reference clock to the feedback clock from the divider and generates the up and down pulse through the charge pump. The charge pump provides current to the loop filter to control the VCO output frequency. The input frequency and output frequency are compared and adjusted through feedback loops until the output frequency equals the input frequency. The VCO and charge pump receive a supply through the regulator. The digital block performs the initial coarse tuning on the VCO to set the initial band close to the target frequency. PLL toggles afterward, and the loop is settled.



*D. Turker et al., "A 7.4-to-14GHz PLL with 54fsrms jitter in 16nm FinFET for integrated RF-data-converter SoCs," in Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, San Francisco, Feb. 2018, pp. 378–380.

Figure 4. The LCPLL circuit [1].

A. FLOW SET UP

In this study, digital blocks of coarse tune are imported into schematic and netlisted together with other analog blocks in the analog design environment. The top-level verification test bench is imported directly from the analog test bench. It is further customized with control registers and logic controls for the RTL blocks. The customization includes importing register settings from CSV files and optimizing the power up and down resetting sequence to speed up the simulation. The simulation is performed inside the analog design environment using the parallel analog SPICE simulator in the VX mode. Simulation results are verified by plotting signal waveforms and evaluating measurement expressions. The simulation time for PLL with multiple modes is reduced from months in the traditional flow to weeks in the new flow. The accuracy of the VX mode is found sufficient for verification of the analog circuit function with RTL code.

B. RESULTS COMPARISON BETWEEN TRADITIONAL FLOW AND THE NEW FLOW

The PLL in our study has 1.2 million nodes, 300 thousand transistors and more than 3 million parasitic capacitors and resistors. Here we discuss one of the verification tasks in detail. In this task a simulation of 100 microseconds is performed. In the VX mode the parallel simulator successfully finished the simulation in 12 days. As a comparison, the traditional digital-analog co-

simulation using a fast SPICE engine was not able to complete the simulation within the time limit allowed by the LSF, and the process was eventually terminated. We want to point out that even with the parallel simulator the VX mode is the only option that was able to complete this simulation, whereas all other modes exceeded the LSF time limit and were terminated as well.

Simulated signal waveforms inside the PLL are plotted in Fig. 5. The first one is the VCO frequency. It exhibits two phases. The first one is the coarse calibration, where the RTL code is toggling. This phase is followed by the fine-tuning phase, which is part of the PLL locking. The RTL code plot for coarse tune shows initial toggling and then converges to the right code to approach a frequency near the target PLL frequency. This indicates that the RTL code is simulated correctly. From the PLL phase plot we can see that vcontrol 1 and 2 are moving and then settling after about 10μs. It confirms that the analog portion of PLL is also working properly in the simulation.

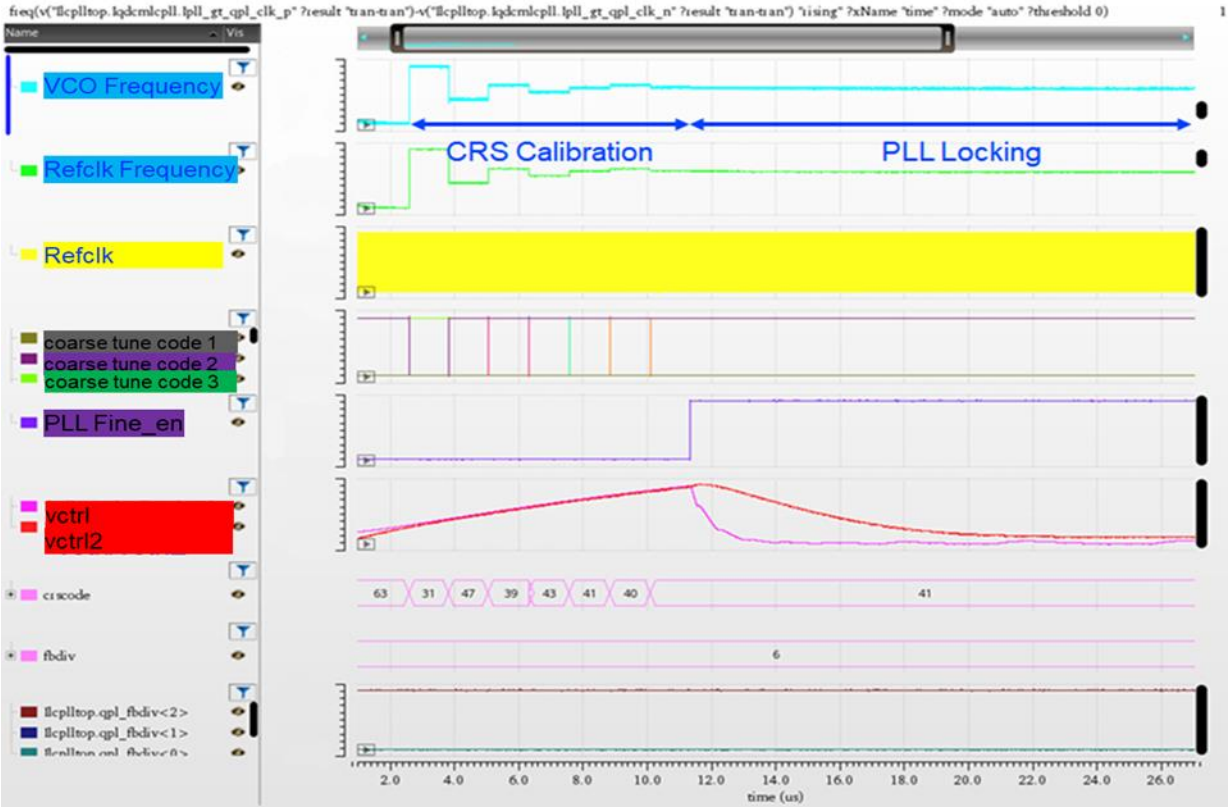


Figure 5. Simulated PLL signal waveforms.

V. SUMMARY

A novel AMS simulation flow is presented. The flow utilizes a single parallel analog SPICE simulator for mixed-signal functional verification in 7nm designs to achieve SPICE-level accuracy.

Both block level simulation and top-level functional verification can be performed in the same schematic based analog design environment, eliminating the need of switching between analog and digital environments required in the traditional AMS co-simulation flow. This flow is proven efficient to detect potential bugs at early design phase. It reduces the design cycle and provides confidence for final sign-off.

References

1. D. Turker et al., “A 7.4-to-14GHz PLL with 54fsrms jitter in 16nm FinFET for integrated RF-data-converter SoCs,” in Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, San Francisco, Feb. 2018, pp. 378–380.